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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,941	10/06/2003	Anuj Gupta	852463.404	3600

500 7590 11/10/2004

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,941	GUPTA ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,9-18 and 20-25* is/are rejected.

7)☒ Claim(s) *4,8 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 10/06/2003.

3. Information disclosed and list on PTO 1449 was considered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

5. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3,5-7,9-18,20-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Proebsting (U.S. Patent No. 5,936,905).

Regarding claim 1, Proebsting discloses a sense amplifier (Figure 2) for a memory array providing increased reliability in sensing small voltage, comprising:

two cross coupled inverters (202/204, 206/208) forming a latch;

supply coupling means for selectively connecting the latch to a supply source (Figure 2, Figure 3, VCC, Column 16-25); and

bit line coupling means (Column 1, lines 54-62) for selectively connecting inputs of each inverter to complimentary bit lines from the memory array; and

delaying means (Column 1, lines 59-60) for delaying the disconnection of the bit lines from the sense amplifier (Figure 2, STRB, Column 4, lines 54-62).

Regarding claims 2-3, 5-7, Proebsting further comprising compensating means for correcting an offset (Column 1, lines 38-46) between the inverters of the latch and the supply coupling means, and wherein the supply coupling means comprise an NMOS transistor (Figure 2, 218),and wherein the compensating means comprise a pair of NMOS transistors (Figure 2, 214,218) connected between the latch and the common supply terminal (Figure 2), and wherein the supply coupling means is controlled by a strobe signal (Figure 2, STRB, Column 1, lines 38-39), and wherein the strobe signal to disable the supply coupling means is delayed by the delaying means (Column 3, lines 26-57).

Regarding claims 13, 18, 20, Proebsting discloses an amplifier (Figure 2) for a memory array, comprising:

a latch circuit (202,204,206,208);

a switch circuit (214, 216, 218) configured to selectively connect inputs of the latch circuit to complementary bit lines from the memory array; and

a delay circuit (Figure 3, STRB, 326) coupled to the switch circuit and configured to delay a disconnection of the bit lines from the latch circuit.

Regarding claims 14-17, Proebsting discloses wherein the latch comprises first and second inverters cross-coupled together (202,204,206,208), and wherein the inverters are formed of CMOS transistors (Figure 2), and further comprising a compensation circuit coupled to the latch and configured to correct for an offset between the inverters of the latch and a supply coupling circuit that selectively connects the latch to a voltage supply source (Column 3, lines 26-57), wherein the delay circuit is configured to generate a delayed enable signal in response to a sense amplifier enable signal (Column 4, lines 50-62).

Regarding claims 9-12, 21-25, the apparatus discussed above would perform the method in claims 21-25.

Allowable Subject Matter

8. Claims 4, 8, 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4,8, 19 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Proebsting (U.S. Patent No. 5,936,905), and others, does not teach

the claimed invention having a PMOS transistor connected in series between each bit and the latch and a delayed sense amplifier means comprises a plurality of inverters connected in series.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER